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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/896,395	06/29/2001	Brian K. Langendorf	42390 P10570	1007

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EXAMINER	
MYERS, PAUL R	

ART UNIT	PAPER NUMBER
2112	

DATE MAILED: 03/02/2004 14

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/896,395	Applicant(s) LANGENDORF ET AL.	
	Examiner Paul R. Myers	Art Unit 2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *13*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference sign(s) not mentioned in the description: 156. A proposed drawing correction, corrected drawings, or amendment to the specification to add the reference sign(s) in the description, are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claims 1-30 rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

In regards to claims 1, 12, 18 and 24: The claim amendment that the virtual PCI device is a device "other than a virtual host-to-PCI bridge". Applicants specification only indicates that the virtual PCI device is some PCI device without indication of what the device is. In fact the specification gives only one example of what the virtual PCI device can be and that example is expressly a virtual PCI-to-PCI bridge. The examiner further notes the virtual host-to-PCI bridge of the 82433BX is a virtual PCI-to-PCI bridge.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-3, 5-6, 9-12, 14-19 and 21-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over the Intel 440BX AGPset: 82443BX Host Bridge Controller. Herein after 82443BX in view of Falardeau et al PN 6,629,157

In regards to claim 1, 12, 18, 21 and 24-25: 82443BX teaches an apparatus comprising: an interface (Page iv Host interface) for directly coupling to a host bus (Host bus) having one or more processors (Page iii multiprocessor support); a device (Page 3-5 "Virtual Host-to-PCI Bridge" identified as device 1 also the AGP interface note 82443BX also has a device 0) coupled to the interface to perform one or more functions (AGP interface functions page 3-1), said device appearing as a virtual PCI device (82443BX calls it virtual) logically residing on a PCI bus (PCI bus 0) that is coupled to the host bus through a host-to-PCI bridge (Host-to-PCI bridge); and a monitor circuit (Decoder Page 1-2) coupled to said interface and said device to track host bus cycles (Host cycles) initiated by at least one of the processors coupled to the host bus, to identify processor initiated host bus cycles targeted to the virtual PCI device and to generate one or more control signals (DEVSEL#) to respond, as the virtual PCI device, to said one or more said identified host bus cycles targeted to said virtual PCI device. The 82443BX virtual PCI device is a virtual PCI-to-PCI device. 82443BX does not expressly teach a virtual PCI device that is a

device "other than a virtual host-to-PCI device". 82443BX does teach the virtual Host-to PCI bridge being attached to an arbitrary AGP/PCI device. Falardeau et al teaches a virtual PCI device that is any arbitrary PCI device. It would have been obvious to a person of ordinary skill in the art to allow the use of any arbitrary virtual PCI device because this would have allowed greater system flexibility.

In regards to claim 2: 82443BX teaches plural storages associated with host bus read and write cycles (Page v-vi Registers) addressed to the virtual PCI device (Device 0 or Device 1).

In regards to claim 3: 82443BX teaches a second storage for storing data transferred to said virtual device (in-order queue).

In regards to claim 5: 82443BX teaches an internal bus.

In regards to claim 6, 16, 30: 82443BX teaches the virtual device being a virtual PCI-to-PCI bridge.

In regards to claim 9, 14: 82443BX teaches I/O address space.

In regards to claims 10-11, 15, 19, 23, 26-27, 29: 82443BX teaches configuration/control registers and configuring.

In regards to claim 17, 22, 28: 82443BX teaches identifying the device and bus number of the virtual device (Device 0 or 1 and PCI bus 0). 82443BX also teaches handling snoop requests.

In regards to claim 4: 82443BX teaches an external processor. 82443BX also teaches said first and second storage, said monitor circuit and said virtual device all being integrated on a single chip. 82443BX does not teach the processor also being integrated on the chip. MPEP

2144.04 V B states barring some unexpected results to make integral is not a patentable distinction.

In regards to claim 7, 13 and 20: 82443BX teaches said storage being registers. Official notice is taken that random access memories are well known in the art. It would have been obvious to use a random access memory because this would have allowed greater storage capacity. 82443BX teaches an array of registers.

6. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over 82433BX in view of Falardeau et al PN 6,629,157 as applied to claim 1 above, and further in view of Huott et al PN 5,659,551.

In regards to claim 8: 82443BX teaches configuration/control registers. 82443BX does not teach mirror registers of these registers. Huott et al teaches the use of mirror registers for mirroring the configuration registers to repair configuration in the case of errors. It would have been obvious to include mirror registers of the configuration because this would have allowed for error correction.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul R. Myers whose telephone number is 703 305 9656. The examiner can normally be reached on Mon-Thur 6:30-4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart can be reached on 703 305 4815. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Paul R. Myers

PRM
February 26, 2004

PAUL R. MYERS
PRIMARY EXAMINER